REMARKS/ARGUMENTS

Claims 1-16 are pending in this application. Claims 4 and 9 have been cancelled. New claims 12-18 have been added to more distinctly claim the invention. Support for the new claims is found in the specification, and no new matter has been added. The abstract has been amended to address the examiner's objection.

Allowable Claims

Claims 1 and 2 are allowable as the examiner indicated. Claim 4 has been rewritten independent form as new claim 12, and this claim should be allowable as the examiner indicated. Claims 13-15 are dependent on claim 12 and should also be allowable. Claim 9 has been rewritten independent form as new claim 16, and this claim should be allowable as the examiner indicated. Claims 16-18 are dependent on claim 16 and should also be allowable.

Claims 3, 5-8, and 10-11

Claims 3, 5-8, and 10-11 were rejected as being unpatentable over U.S. patent 6,070,003 issued to Gove et al. (Gove) in view of general skill of a worker in the art. Reconsideration and allowance of claims are respectfully requested for the following reasons.

Claims 3 and 8 recite "a processor switch chip having a plurality of processors each connected to a processor crossbar" and "a memory switch chip having a plurality of memory controllers each connected to a memory crossbar and controlling a shared memory bank."

Gove does not show or suggest a processor crossbar and a memory crossbar, which the examiner confirms. Gove provides no suggestion that a cycle-rate local connection network (crossbars) 20 (in figure 1) should be divided into a processor crossbar and a memory crossbar as recited. In fact, Gove teaches quite the opposite when stating "the entire image processor, including the individual processors, the crossbar switch and the memories, is contained on a single silicon chip." See abstract. Furthermore, the summary, at column 3, lines 12-22, states "the crossbar switch is constructed . . . so as to conserve space." Gove is trying to

minimize circuitry and would not have a processor crossbar and a memory crossbar, because these take more space. For at least this reason, there is no suggestion to combine Gove in view of general skill of a worker in the art in such as way to show or suggest the invention as recited in claims 3 and 8.

Furthermore, in the invention, the memory switch chip has "a plurality of memory controllers." This is not shown or suggested by Gove. More specifically, in figure 64, processors are denoted by reference numbers 100 to 103, and memories and denoted by reference number 10. There is a crossbar switch 20 between the processors and memories. Gove has no memory controllers in memories 10. Controller 3002 is a program flow control unit controller operation of the processor, not a memory controller as recited in the claims. Therefore, for at least this additional reason, Gove in view of general skill of a worker in the art does not show or suggest the invention as recited in claims 3 and 8.

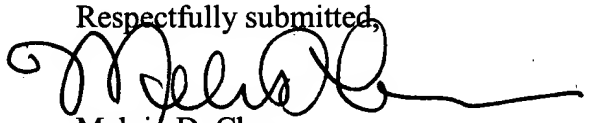
Claims 5-7 are dependent on claim 3 and should be allowable for at least similar reasons as discussed above. Claims 10 and 11 are dependent on claim 8 and should be allowable for at least similar reasons as discussed above.

CONCLUSION

In view of the foregoing, applicants believe all claims now pending in this application are in condition for allowance. The issuance of a formal notice of allowance at an early date is respectfully requested.

If the examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400, extension 5213.

Respectfully submitted,



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